detection, said first power-on detection circuit performing detection of the power-on independently of a voltage level of the second power supply voltage;

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a main power-on detection circuit coupled to the first and second power-on detection circuits for generating a main power-on detection signal rendered active from activation of a first activated power-on detection signal of the first and second power-on detection signals until inactivation of a second activated power-on detection signal of the first and second power-on detection signals.

11. (TWICE AMENDED) A semiconductor integrated circuit device comprising;

an internal voltage generation circuit receiving a first power supply voltage and generating, from said first power supply voltage, an internal voltage different in voltage level from said first power supply voltage;

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an internal voltage application detection circuit for activating an internal voltage power-up detection signal according to a voltage level of said internal voltage;

a power-on detection circuit for detecting power-on of a second power supply voltage independently of a voltage level of said internal voltage, to activate a power-on detection signal according to a result of detection, said internal voltage application detection circuit performing detection of the voltage level of the internal voltage independently of a voltage level of the second power supply voltage; and

a main power-on detection circuit responsive to said internal voltage power-up detection signal and said power-on detection signal for generating a main power-on detection signal rendered active from activation of a first activated detection signal of the internal voltage power-up detection signal and the power-on detection signal until inactivation of second activated

detection signal of the internal voltage power-up detection signal and the power-on detection signal.

19. (TWICE AMENDED) A semiconductor device receiving a plurality of power supply voltages for operation, comprising:

a plurality of power-up detection circuits provided for the respective power supply voltages and detecting power-up of the respective power supply voltages to generate power-up detection signals corresponding to the respective power supply voltages, each power-up detection circuit detecting a voltage level of a corresponding power supply voltage independently of a voltage level of the power supply voltage other than the corresponding power supply voltage; and

a main power-on detection circuit coupled to receive the respective power supply voltages for activating a main power-on detection signal from activation of a first activated power-up detection signal in the power-up detection signals until inactivation of a last activated power-up detection signal in the power-up detection signals, to hold an internal circuit in a reset state.

20. (TWICE AMENDED) A semiconductor device comprising:

internal voltage generation circuitry coupled to receive at least one power supply voltage and generating, from said at least one power supply voltage, a plurality of internal voltages differing in voltage level from each other;

internal voltage power-up detection circuitry provided for at least one of the plurality of internal voltages and detecting power-up of the at least one internal voltage in accordance with a

voltage level of said at least one internal voltage for generating at least one internal voltage power-up detection signal for said at least one internal voltage;

power-on detection circuitry provided for at least one power source voltage other than said at least one power supply voltage, for detecting power-on of said at least one power source voltage in accordance with a voltage level of said at least one power source voltage independently of the voltage level of said at least one internal voltage, to generate at least one power-on detection signal for the respective at least one power source voltage, said internal voltage power-up detection circuitry performing detection independently of the voltage level of the at least one power source voltage; and

main power-on detection circuitry responsive to said at least one internal voltage power-up detection signal and said at least one power-on detection signal for generating a main power-on detection signal made active from activation of a first activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal until inactivation of a last activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal, to hold an internal circuit in a reset state.

Please add new claims 21-24 as follows:

21. (NEW) The semiconductor integrated device according to claim 1, wherein the activation of the detection signal indicates instability of a corresponding power supply voltage, and the inactivation of the detection signal indicates stability of the corresponding power supply voltage.

22. (NEW) The semiconductor integrated circuit device according to claim 11, wherein activation of the detection signal indicates instability of a corresponding power supply voltage, and inactivation of the detection signal indicates stability of the corresponding power supply voltage.

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23. (NEW) The semiconductor device according to claim 19, wherein the activation of the detection signal indicates instability of a corresponding power supply voltage, and the inactivation of the detection signal indicates stability of the corresponding power supply voltage.

24. (NEW) The semiconductor device according to claim 20, wherein the activation of the detection signal indicates instability of a corresponding voltage and the inactivation of the detection signal indicates stability of the corresponding voltage.